**LESSION PLAN**

**NAME OF THE FACULTY** : - Manju

**DISCIPLINE** : - ECE

**SEMESTER** : - FOURTH

**SUBJECT** : - MPD

**LESSON PLAN DURATION** : - 15 weeks (From 06 March 2023 to 23 June 2023)

Work load (lecture/practical) per week (in hours):- lecture-**03** /practical-**03** hrs per group

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| **WEEK** | **THEORY** | | **PRACTICAL** | |
| **LECTURE DAY** | **TOPIC**  **(including assignment/test)** | **PRACTICAL DAY** | **TOPIC** |
| 1st | 1st | **Evolution of Microprocessor**:  Typical organization of a microcomputer system and functions of its various blocks. | 1st  Group-1 | Familiarization of different keys of 8085 microprocessor kit and its memory map |
| 2nd | Typical organization of a microcomputer system and functions of its various blocks. |  |  |
| 3rd | Microprocessor:- its evolution & function | 2nd  Group-2 | Familiarization of different keys of 8085 microprocessor kit and its memory map |
| 2nd | 4th | Microprocessor:- its impact on modern society | 3rd  Group-1 | Steps to enter, modify data/program and to execute a programme on 8085 kit |
| 5th | **Architecture of a Microprocessor**  (With reference to 8085 microprocessor)  :- Introduction |  |  |
| 6th | Concept of Bus | 4th  Group-2 | Steps to enter, modify data/program and to execute a programme on 8085 kit |
| 3rd | 7th | Bus organization of 8085 | 5th  Group-1 | Writing and execution of ALP for addition and substation of two 8 bit numbers |
| 8th | Functional block diagram of 8085 |  |  |
| 9th | Pin details of 8085 and related signals | 6th  Group-2 | Writing and execution of ALP for addition and substation of two 8 bit numbers |
| 4th | 10th | Demultiplexing of address/data bus generation of read/write control signals | 7th  Group-1 | **Revision** |
| 11th | Demultiplexing of address/data bus generation of read/write control signals |  |  |
| 12th | Steps to execute a stored programme | 8th  Group-2 | **Revision** |
| 5th | 13th | **Assignment-1** | 9th  Group-1 | Writing and execution of ALP for multiplication and division of two 8 bit numbers |
| 14th | **Class Test-1** |  |  |
| 15th | Instruction Timing and Cycles Introduction | 10th  Group-2 | Writing and execution of ALP for multiplication and division of two 8 bit numbers |
| 6th | 16th | Instruction cycle, Machine cycle | 11th  Group-1 | Writing and execution of ALP for arranging 10 numbers in ascending/descending order |
| 17th | T-states |  |  |
| 18th | Fetch and execute cycle. | 12th  Group-2 | Writing and execution of ALP for arranging 10 numbers in ascending/descending order |
| 7th | 19th | Fetch and execute cycle. | 13th  Group-1 | Writing and execution of ALP for 0 to 9 BCD counters (up/down counter according to choice stored in memory) |
| 20th | . **Programming (with respect to 8085 microprocessor)** :- Introduction |  |  |
| 21th | Brief idea of machine and assembly languages | 14th  Group-1 | Writing and execution of ALP for 0 to 9 BCD counters (up/down counter according to choice stored in memory) |

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| 8th | 22th |  | 15th  Group-1 | **Revision** |
| 23th | Instruction format and Addressing mode |  |  |
| 24th | Identification of instructions as to which addressing mode they belong | 16th  Group-2 | **Revision** |
| 9th | 25th | Concept of Instruction set | 17th  Group-1 | Interfacing exercise on 8255 like LED display control |
| 26th | Explanation of the instructions of the following groups of instruction set |  |  |
| 27th | Data transfer group, Arithmetic Group, Logic Group, Stack, I/O and Machine Control Group | 18th  Group-2 | Interfacing exercise on 8255 like LED display control |
| 10th | 28th | Data transfer group, Arithmetic Group, Logic Group, Stack, I/O and Machine Control Group | 19th  Group-1 | Interfacing exercise on 8253 programmable interval timer |
| 29th | Programming exercises in assembly language. (Examples can be taken from the list of experiments). |  |  |
| 30th | Programming exercises in assembly language. (Examples can be taken from the list of experiments). | 20th  Group-2 | Interfacing exercise on 8253 programmable interval timer |
| 11th | 31th | Memories and I/O interfacing:- Introduction | 21th  Group-1 | Interfacing exercise on 8279 programmable KB/display interface like to display the hex code of key pressed on display |
| 32th | Concept of memory mapping, partitioning of total memory space, Address decoding |  |  |
| 33th | Concept of peripheral mapped I/O and memory mapped I/O , Interfacing of memory mapped I/O devices | 22th  Group-2 | Interfacing exercise on 8279 programmable KB/display interface like to display the hex code of key pressed on display |
| 12th | 34th | **Assignment-2** | 23th  Group-1 | **Revision** |
| 35th | **Class test-2** |  |  |
| 36th | **Interrupts**:- Concept of interrupt, Maskable and non-maskable, Edge triggered and level triggered interrupts, Software interrupt, Restart interrupts and its use. | 24th  Group-2 | **Revision** |
| 13th | 37th | Various hardware interrupts of 8085, Servicing interrupts, extending interrupt system | 25th  Group-1 | Use of 8085 emulator for hardware testing |
| 38th | Data Transfer Techniques:- Concept of programmed I/O operations, |  |  |
| 39th | sync data transfer, async data transfer (hand shaking), | 26th  Group-2 | Use of 8085 emulator for hardware testing |
| 14th | 40th | Interrupt driven data transfer, DMA, Serial output data, Serial input data | 27th  Group-1 | **Revision** |
| 41th | **Peripheral devices:-** 8255 PPI, 8253 PIT and |  |  |
| 42th | 8257 DMA controller | 28th  Group-2 | **Revision** |
| 15th | 43th | Architecture of 8086 Microprocessor:-  Block diagram | 29th  Group-1 | **Viva** |
| 44th | Architecture of 8086 Microprocessor :-  Minimum and Maximum mode  Pin and Signals  **Assignment-3** |  |  |
| 45th | **class test-3** | 30th  Group-2 | **Viva** |